

REMARKS**Claim Rejections Under 35 U.S.C. § 102**

Claims 1-23 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Fastow et al.* (U.S. Patent No. 6,583,479). Applicant respectfully traverses this rejection.

Claim 1 has been amended to add the subject matter of claim 2. Claim 2 has been canceled without prejudice to avoid duplication. Claim 20 has been amended to include the subject matter of claims 21 – 23. Claims 21 – 23 have been canceled without prejudice to avoid duplication.

Fastow et al. discloses an NROM memory transistor for use in a memory array. The Examiner states that the negative bias connection to the substrate, as claimed in the present claims, is present in *Fastow et al.* However, Applicant can find neither a teaching nor a suggestion regarding a negative substrate bias in the specification or the drawings.

Fastow et al. also neither teaches nor suggests a vertical memory cell that has both a high-k gate insulator and a negative bias connection to the substrate to enhance hot electron injection as claimed in the present claims. Additionally, *Fastow et al.* neither teaches nor suggests a composite gate insulator that is comprised of two or more oxide materials selected from the group of silicon, titanium, tantalum, hafnium, and lanthanum.

Double Patenting Rejection

Claims 1-23 were provisionally rejected under the judicially created obviousness-type double patenting as being unpatentable over claims 1-64 of copending U.S. Patent Application Serial No. 10/177,208. Applicant respectfully traverses this provisional rejection.

The claims of U.S. Patent Application Serial No. 10/177,208 do not include limitations to high-k gate insulator, composite gate insulator, or negative bias connection on substrate as is claimed in the present claims. These are non-obvious variations of the invention claimed in copending application 10/177,208. Therefore, Applicant does not believe that a terminal disclaimer is required in the present application.

CONCLUSION

For the above-described reasons, the Applicant believes that claims 1 and 3 – 20 of the present application are in condition for allowance. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

Date: _____

11/10/05

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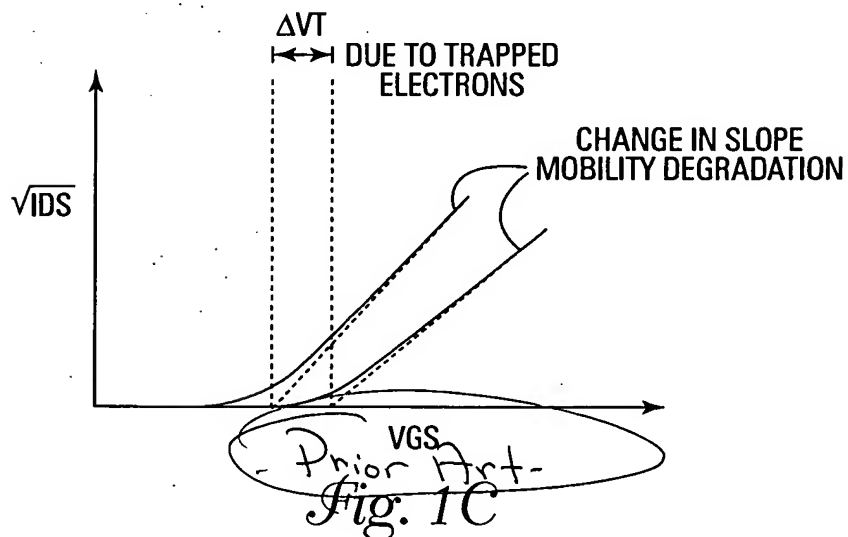
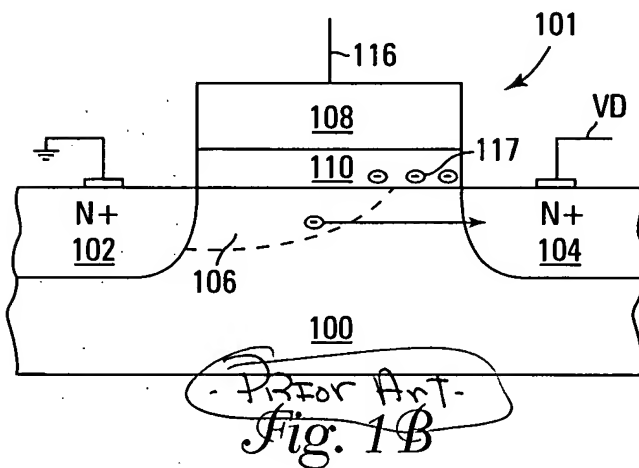
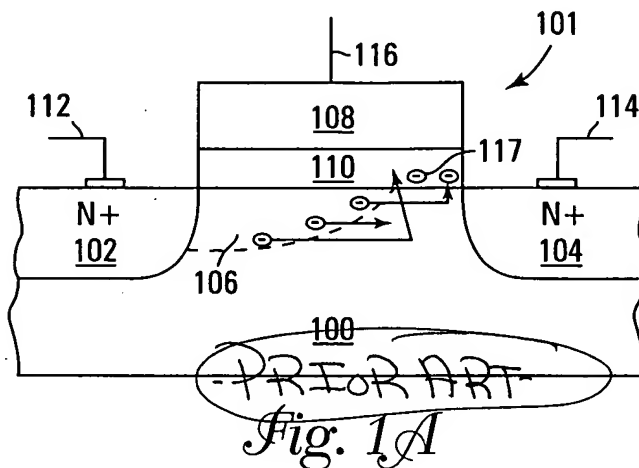
AMENDMENTS TO THE DRAWINGS

Figures 1A, 1B 1C and 6 have been amended to add the prior art legend. The amendments are shown in the replacement annotated marked-up drawing sheets and are included in the attached replacement sheets.



ANNOTATED MARKED-UP DRAWING
Inventor: Leonard Forbes
VERTICAL NROM HAVING STORAGE DENSITY OF 1 BIT PER 1F2
Atty Docket No. 400.250US01

1/8



6/8

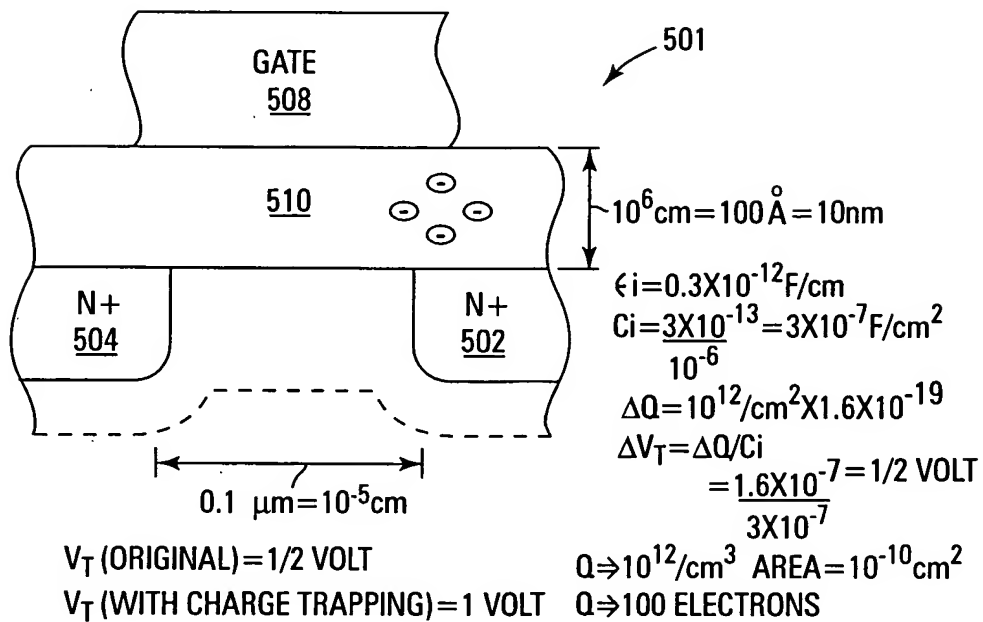


Fig. 5A

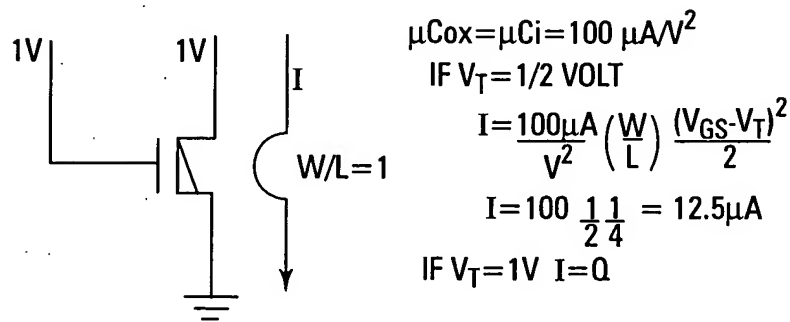


Fig. 5B

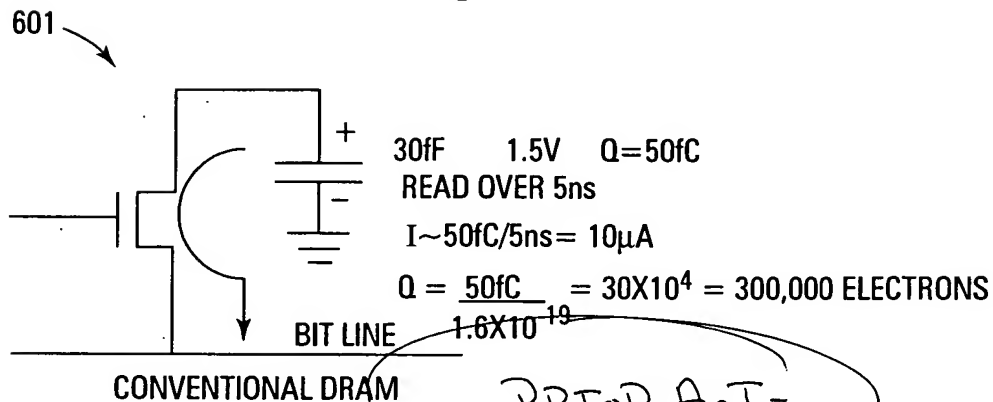


Fig. 6

- PRIOR ART -